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RTL8370N-VB-CG

LAYER 2 MANAGED 8-PORT 10/100/1000 SWITCH CONTROLLER

DRAFT DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8370N-VB ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2013/8/20	First release.
0.2	2014/9/15	Revise some description and error.
0.3	2015/8/4	Revise some description and error. Delete chapter Register Description. Add chapter 7.4 Serial Mode LED Pins, 10.4 SPI FLASH Interface, 11.5.4 Serial Shift Mode LED Interface Timing Characteristics, and 11.5.5 SPI FLASH Interface Timing Characteristics.

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1. General Description

The RTL8370N-VB is an LQFP128 E-PAD, high-performance 8-port Gigabit Ethernet switch. The RTL8370N-VB features low-power integrated 8-port Giga-PHYs that support 1000Base-T, 100Base-T, and 10Base-T.

The embedded packet storage SRAM in the RTL8370N-VB features superior memory management technology to efficiently utilize memory space. The RTL8370N-VB integrates a 4096-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the Slave I^2C-like interface or Slave MII Management interface, and each of the entries can be configured as a static entry. The entry aging time is between 200 and 400 seconds. Eight Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The RTL8370N-VB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8370N-VB supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8370N-VB can forward IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping protocol packets.

In order to support flexible traffic classification, the RTL8370N-VB supports 96-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8370N-VB supports 16 sets and four statuses: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol.

To meet security and management application requirements, the RTL8370N-VB supports IEEE 802.1x Port-based/MAC-based Access Control. For those ports that do not pass IEEE 802.1x authentication, the RTL8370N-VB provides a Port-based/MAC-based Guest VLAN function for them to access limited network resources. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time or multimedia networking applications, the RTL8370N-VB supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority; (5) CVLAN-based priority; (6) SVLAN-based priority; and (7) SMAC-based/LUTFWD-based priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8370N-VB provides a 4096-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8370N-VB

supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology.

In embedded system applications, CPU may want to know the input port of the incoming packet. The RTL8370N-VB supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8370N-VB also provides an option to admit VLAN tagged packet with a specific PVID only. If this function is enabled, the RTL8370N-VB will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- RTL8370N-VB: Single-chip 8-port gigabit non-blocking switch architecture
- Embedded 8-port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Supports Realtek Cable Test (RTCT) function
- Supports 96-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions support mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment
  - Supports 5 types of user defined ACL rule format for 64 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4K VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Supports Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Supports per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - Supports 4096-entry MAC address table with 4-way hash algorithm
  - Up to 4096 L2/L3 Filtering Database
- Supports Spanning Tree port behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Supports Quality of Service (QoS)
  - Supports per port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ) to provide minimum bandwidth

- One leaky bucket to constrain the average packet rate of each queue

- Supports rate limiting (64 shared meters, with 8kpbs granulation)

- Supports RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)

- Supports Stacking VLAN and Port Isolation with 8 Enhanced Filtering Databases

- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports 32 L2/IPv4 Multicast mappings to SVLAN

- Supports 4 IEEE 802.3ad Link aggregation port groups

- Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol

- Supports Loop Detection

- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port

- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers

- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving

- Each port supports 3 parallel LED or scan LED or serial shift LED outputs

- Supports I^2C-like Slave interface or Slave MII Management interface to access configuration register

- Supports 16K-byte EEPROM space for configuration

- Integrated 8051 microprocessor

- Supports SPI Flash Interface

- 25MHz crystal input

- RTL8370N-VB: LQFP 128-pin E-PAD package

3. System Applications

- 8-Port 1000Base-T Switch

4. Application Examples

4.1. 8-Port 1000Base-T Switch

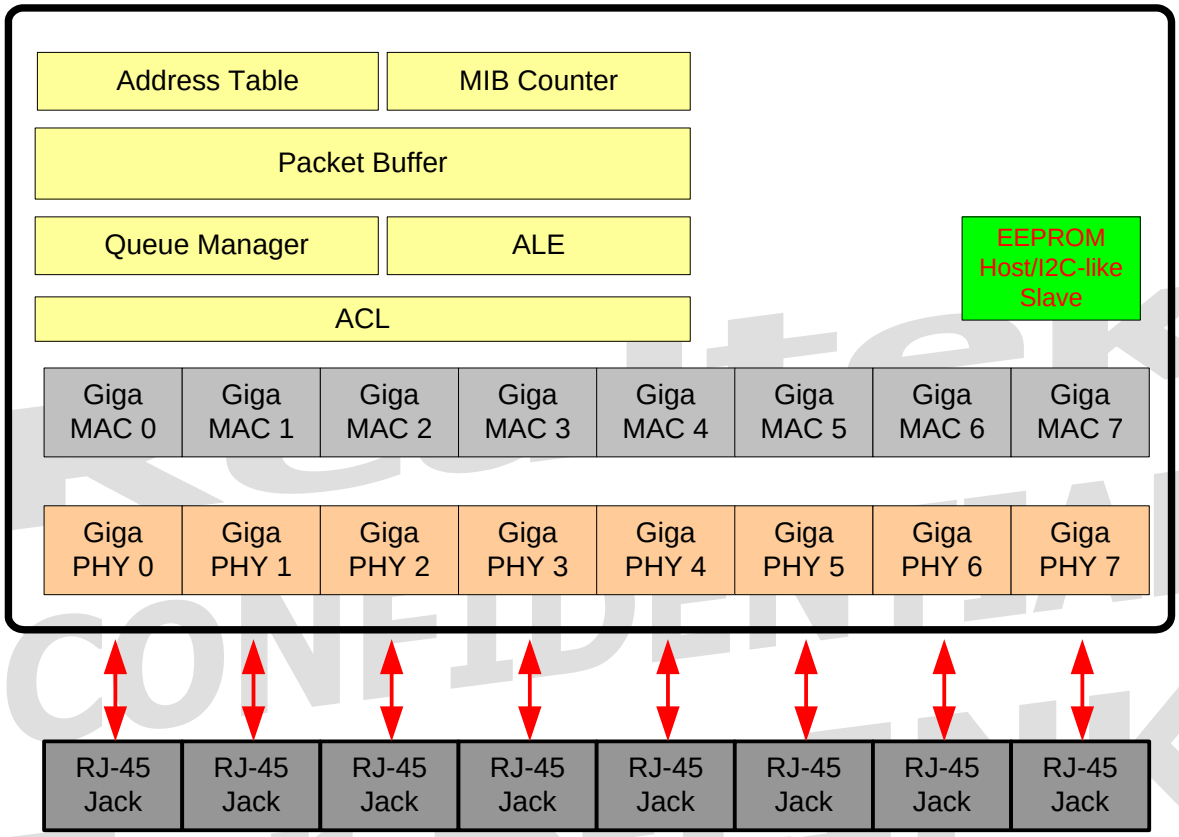


Figure 1. 8-Port 1000Base-T Switch

5. Block Diagram

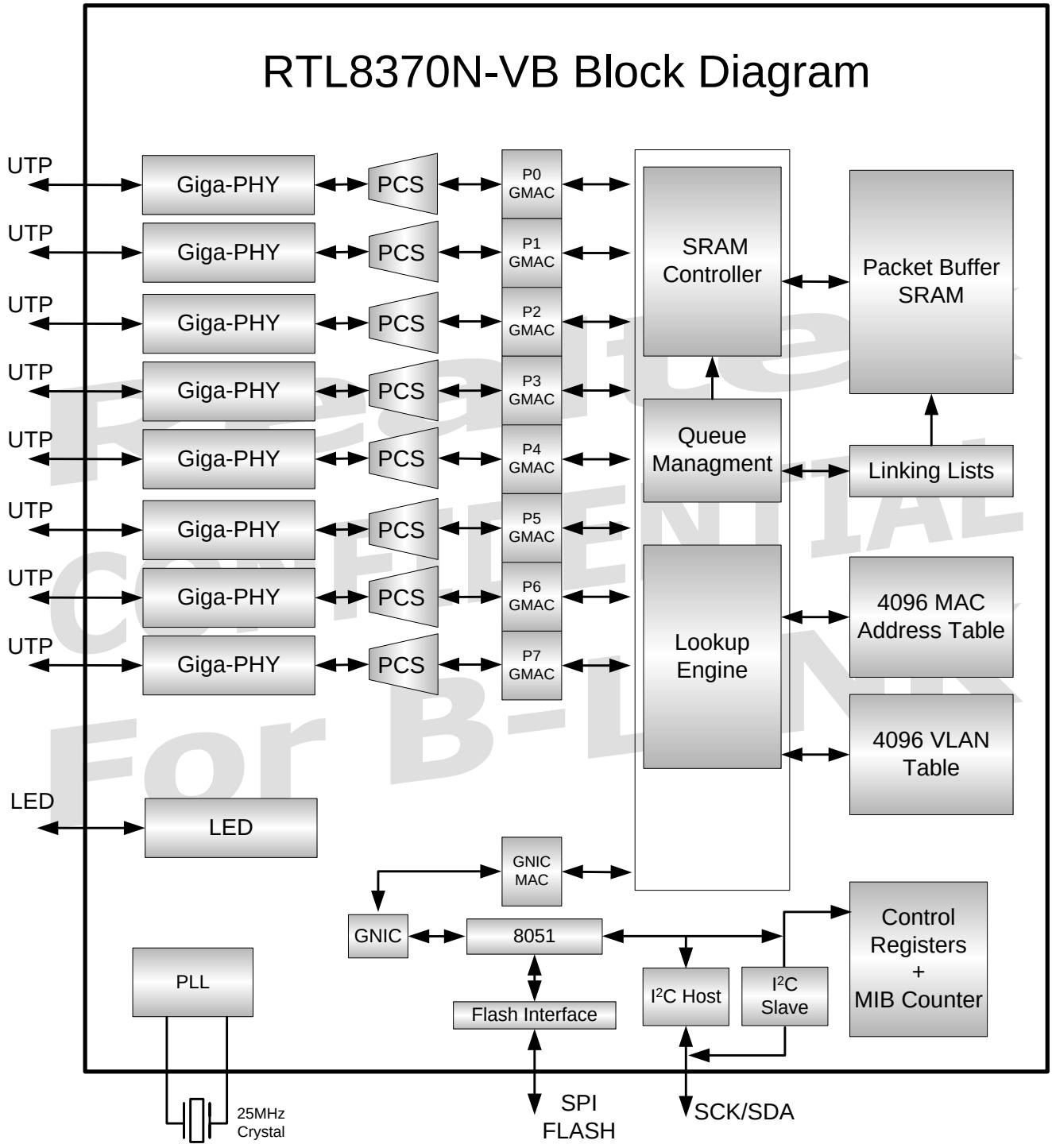


Figure 2. RTL8370N-VB Block Diagram

6. Pin Assignments

6.1. Pin Assignments

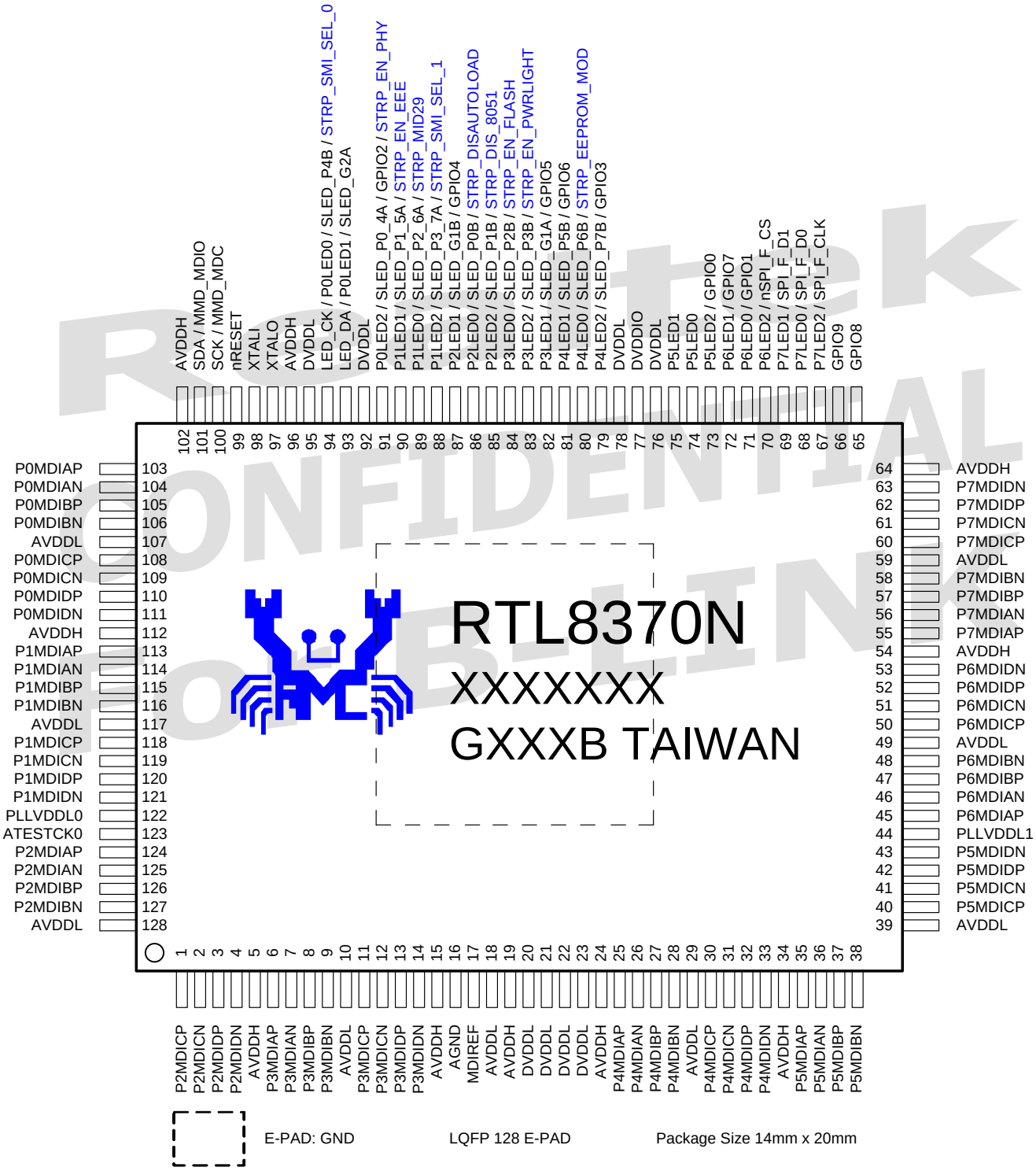


Figure 3. RTL8370N-VB Pin Assignments

6.2. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 3).

6.3. Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

I_{PD}: Input Pin With Pull-Down Resistor; (Typical Value = 75K Ohm)

I_S: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

O_{PD}: Output Pin With Pull-Down Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type
P2MDICP	1	AI/O
P2MDICN	2	AI/O
P2MDIDP	3	AI/O
P2MDIDN	4	AI/O
AVDDH	5	AP
P3MDIAP	6	AI/O
P3MDIAN	7	AI/O
P3MDIBP	8	AI/O
P3MDIBN	9	AI/O
AVDDL	10	AP
P3MDICP	11	AI/O
P3MDICN	12	AI/O
P3MDIDP	13	AI/O
P3MDIDN	14	AI/O
AVDDH	15	AP
AGND	16	AG
MDIREF	17	AO

Name	Pin No.	Type
AVDDL	18	AP
AVDDH	19	AP
DVDDL	20	P
DVDDL	21	P
DVDDL	22	P
DVDDL	23	P
AVDDH	24	AP
P4MDIAP	25	AI/O
P4MDIAN	26	AI/O
P4MDIBP	27	AI/O
P4MDIBN	28	AI/O
AVDDL	29	AP
P4MDICP	30	AI/O
P4MDICN	31	AI/O
P4MDIDP	32	AI/O
P4MDIDN	33	AI/O
AVDDH	34	AP

Name	Pin No.	Type
P5MDIAP	35	AI/O
P5MDIAN	36	AI/O
P5MDIBP	37	AI/O
P5MDIBN	38	AI/O
AVDDL	39	AP
P5MDICP	40	AI/O
P5MDICN	41	AI/O
P5MDIDP	42	AI/O
P5MDIDN	43	AI/O
PLLVDDL1	44	AP
P6MDIAP	45	AI/O
P6MDIAN	46	AI/O
P6MDIBP	47	AI/O
P6MDIBN	48	AI/O
AVDDL	49	AP
P6MDICP	50	AI/O
P6MDICN	51	AI/O
P6MDIDP	52	AI/O
P6MDIDN	53	AI/O
AVDDH	54	AP
P7MDIAP	55	AI/O
P7MDIAN	56	AI/O
P7MDIBP	57	AI/O
P7MDIBN	58	AI/O
AVDDL	59	AP
P7MDICP	60	AI/O
P7MDICN	61	AI/O
P7MDIDP	62	AI/O
P7MDIDN	63	AI/O
AVDDH	64	AP
GPIO8	65	I/O_{PU}
GPIO9	66	I/O_{PU}
P7LED2/SPI_F_CLK	67	I/O_{PU}
P7LED0/SPI_F_D0	68	I/O_{PU}
P7LED1/SPI_F_D1	69	I/O_{PU}
P6LED2/nSPI_F_CS	70	I/O_{PU}
P6LED0/GPIO1	71	I/O_{PU}
P6LED1/GPIO7	72	I/O_{PU}
P5LED2/GPIO0	73	I/O_{PU}
P5LED0	74	I/O_{PU}
P5LED1	75	I/O_{PU}
DVDDL	76	P
DVDDIO	77	P
DVDDL	78	P

Name	Pin No.	Type
P4LED2/SLED_P7B/GPIO3	79	I/O_{PU}
P4LED0/SLED_P6B/ STRP_EEPROM_MOD	80	I/O_{PU}
P4LED1/SLED_P5B/GPIO6	81	I/O_{PU}
P3LED1/SLED_G1A/GPIO5	82	I/O_{PU}
P3LED2/SLED_P3B/ STRP_EN_PWRLIGHT	83	I/O_{PU}
P3LED0/SLED_P2B/ STRP_EN_FLASH	84	I/O_{PU}
P2LED2/SLED_P1B/ STRP_DIS_8051	85	I/O_{PU}
P2LED0/SLED_P0B/ STRP_DISAUTOLOAD	86	I/O_{PU}
P2LED1/SLED_G1B/GPIO4	87	I/O_{PU}
P1LED2/SLED_P3_7A/ STRP_SMI_SEL_1	88	I/O_{PU}
P1LED0/SLED_P2_6A/ STRP_MID29	89	I/O_{PU}
P1LED1/SLED_P1_5A/STRP_EN _EEE	90	I/O_{PU}
P0LED2/SLED_P0_4A/GPIO2/ STRP_EN_PHY	91	I/O_{PU}
DVDDL	92	P
LED_DA/P0LED1/SLED_G2A	93	I/O_{PU}
LED_CK/P0LED0/SLED_P4B/ STRP_SMI_SEL_0	94	I/O_{PU}
DVDDL	95	P
AVDDH	96	AP
XTALO	97	AO
XTALI	98	AI
nRESET	99	I_S
SCK/MMD_MDC	100	I/O_{PU}
SDA/MMD_MDIO	101	I/O_{PU}
AVDDH	102	AP
P0MDIAP	103	AI/O
P0MDIAN	104	AI/O
P0MDIBP	105	AI/O
P0MDIBN	106	AI/O
AVDDL	107	AP
P0MDICP	108	AI/O
P0MDICN	109	AI/O
P0MDIDP	110	AI/O
P0MDIDN	111	AI/O
AVDDH	112	AP
P1MDIAP	113	AI/O
P1MDIAN	114	AI/O

Name	Pin No.	Type
P1MDIBP	115	AI/O
P1MDIBN	116	AI/O
AVDDL	117	AP
P1MDICP	118	AI/O
P1MDICN	119	AI/O
P1MDIDP	120	AI/O
P1MDIDN	121	AI/O
PLLVDDL0	122	AP

Name	Pin No.	Type
ATESTCK0	123	AO
P2MDIAP	124	AI/O
P2MDIAN	125	AI/O
P2MDIBP	126	AI/O
P2MDIBN	127	AI/O
AVDDL	128	AP
GND	EPAD	G

7. Pin Descriptions

7.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	103 104 105 106 108 109 110 111	AI/O	10	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	113 114 115 116 118 119 120 121	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	124 125 126 127 1 2 3 4	AI/O	10	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	6 7 8 9 11 12 13 14	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	25 26 27 28 30 31 32 33	AI/O	10	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

Pin Name	Pin No.	Type	Drive (mA)	Description
P5MDIAP/N P5MDIBP/N P5MDICP/N P5MDIDP/N	35 36 37 38 40 41 42 43	AI/O	10	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P6MDIAP/N P6MDIBP/N P6MDICP/N P6MDIDP/N	45 46 47 48 50 51 52 53	AI/O	10	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P7MDIAP/N P7MDIBP/N P7MDICP/N P7MDIDP/N	55 56 57 58 60 61 62 63	AI/O	10	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

7.2. Parallel LED Pins

Table 3. Parallel LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P7LED2/ SPI_F_CLK	67	I/O_{PU}	-	Port 7 LED2 Output Signal. P7LED2 indicates information is defined by register or EEPROM.
P7LED0/ SPI_F_D0	68	I/O_{PU}	-	Port 7 LED0 Output Signal. P7LED0 indicates information is defined by register or EEPROM.
P7LED1/ SPI_F_D1	69	I/O_{PU}	-	Port 7 LED1 Output Signal. P7LED1 indicates information is defined by register or EEPROM.
P6LED2/ nSPI_F_CS	70	I/O_{PU}	-	Port 6 LED2 Output Signal. P6LED2 indicates information is defined by register or EEPROM.
P6LED0/GPIO1	71	I/O_{PU}	-	Port 6 LED0 Output Signal. P6LED0 indicates information is defined by register or EEPROM.
P6LED1/GPIO7	72	I/O_{PU}	-	Port 6 LED1 Output Signal. P6LED1 indicates information is defined by register or EEPROM.
P5LED2/GPIO0	73	I/O_{PU}	-	Port 5 LED2 Output Signal. P5LED2 indicates information is defined by register or EEPROM.

Pin Name	Pin No.	Type	Drive (mA)	Description
P5LED0	74	I/O_{PU}	-	Port 5 LED0 Output Signal. P5LED0 indicates information is defined by register or EEPROM.
P5LED1	75	I/O_{PU}	-	Port 5 LED1 Output Signal. P5LED1 indicates information is defined by register or EEPROM.
P4LED2	79	I/O_{PU}	-	Port 4 LED2 Output Signal. P4LED2 indicates information is defined by register or EEPROM.
P4LED0/ STRP_EEPROM_MOD	80	I/O_{PU}	-	Port 4 LED0 Output Signal. P4LED0 indicates information is defined by register or EEPROM.
P4LED1/GPIO6	81	I/O_{PU}	-	Port 4 LED1 Output Signal. P4LED1 indicates information is defined by register or EEPROM.
P3LED1/GPIO5	82	I/O_{PU}	-	Port 3 LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM.
P3LED2/ STRP_EN_PWRLIGHT	83	I/O_{PU}	-	Port 3 LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM.
P3LED0/ STRP_EN_FLASH	84	I/O_{PU}	-	Port 3 LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM.
P2LED2/ STRP_DIS_8051	85	I/O_{PU}	-	Port 2 LED2 Output Signal. P2LED2 indicates information is defined by register or EEPROM.
P2LED0/ STRP_DISAUTOLOAD	86	I/O_{PU}	-	Port 2 LED0 Output Signal. P2LED0 indicates information is defined by register or EEPROM.
P2LED1/GPIO4	87	I/O_{PU}	-	Port 2 LED1 Output Signal. P2LED1 indicates information is defined by register or EEPROM.
P1LED2/ STRP_SMI_SEL_1	88	I/O_{PU}	-	Port 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM.
P1LED0/ STRP_MID29	89	I/O_{PU}	-	Port 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM.
P1LED1/ STRP_EN_EEE	90	I/O_{PU}	-	Port 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM.
P0LED2/GPIO2/ STRP_EN_PHY	91	I/O_{PU}	-	Port 0 LED2 Output Signal. P0LED2 indicates information is defined by register or EEPROM.
P0LED1/ LED_DA	93	I/O_{PU}	-	Port 0 LED1 Output Signal. P0LED1 indicates information is defined by register or EEPROM.
P0LED0/ LED_CK/ STRP_SMI_SEL_0	94	I/O_{PU}	-	Port 0 LED0 Output Signal. P0LED0 indicates information is the same as P7LED0 and is defined by register or EEPROM.

7.3. Scan Mode LED Pins

Table 4. Scan Mode LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SLED_G1A/P3LED1 /GPIO5	82	I/O_{PU}	-	Scan Mode LED Group A G1A Output Signal.
SLED_G2A/LED_DA /P0LED1	93	I/O_{PU}	-	Scan Mode LED Group A G2A Output Signal.
SLED_P0_4A/GPIO2 /STRP_EN_PHY/ P0LED2	91	I/O_{PU}	-	Scan Mode LED Group A P0_4A Output Signal.
SLED_P1_5A /P1LED1/ STRP_EN_EEE	90	I/O_{PU}	-	Scan Mode Group A LED P1_5A Output Signal.
SLED_P2_6A/ P1LED0/ STRP_MID29	89	I/O_{PU}	-	Scan Mode LED Group A P2_6A Output Signal.
SLED_P3_7A /P1LED2/ STRP_SMI_SEL_1	88	I/O_{PU}	-	Scan Mode LED Group A P3_7A Output Signal.
SLED_G1B/P2LED1 /GPIO4	87	I/OPU	-	Scan Mode LED Group B G1B Output Signal.
SLED_P0B/P2LED0 /STRP_DISAUTOLOAD	86	I/O_{PU}	-	Scan Mode LED Group B P0B Output Signal.
SLED_P1B/P2LED2 /STRP_DIS_8051	85	I/O_{PU}	-	Scan Mode LED Group B P1B Output Signal.
SLED_P2B/P3LED0/ STRP_EN_FLASH	84	I/O_{PU}	-	Scan Mode LED Group B P2B Output Signal.
SLED_P3B/P3LED2/ STRP_EN_PWRLIGHT	83	I/O_{PU}	-	Scan Mode LED Group B P3B Output Signal.
SLED_P4B/LED_CK /P0LED0/ STRP_SMI_SEL_0	94	I/O_{PU}	-	Scan Mode LED Group B P4B Output Signal.
SLED_P5B/P4LED1 /GPIO6	81	I/O_{PU}	-	Scan Mode LED Group B P5B Output Signal.
SLED_P6B/P4LED0 /STRP_EEPROM_MOD	80	I/O_{PU}	-	Scan Mode LED Group B P6B Output Signal.
SLED_P7B/P4LED2 /GPIO3	79	I/O_{PU}	-	Scan Mode LED Group B P7B Output Signal.

Note: See section 9.19.2 Scan LED Mode, page 34 for details.

7.4. Serial Mode LED Pins

Table 5. Serial Mode LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_DA/ P0LED1	93	I/O_{PU}	-	Serial Shift Mode LED Data Signal.
LED_CK/P0LED0/ STRP_SMI_SEL_0	94	I/O_{PU}	-	Serial Shift Mode LED Clock Signal.

7.5. SPI Flash Pins

Table 6. Test Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
nSPI_F_CS/P6LED2	70	I/O_{PU}	8	SPI FLASH chip select signal.
SPI_F_D1/P7LED1	69	I/O_{PU}	8	In Serial I/O Mode SPI Serial FLASH Serial Data Output (RTL8370N-VB input pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is MSB)
SPI_F_D0/P7LED0	68	I/O_{PU}	8	In Serial I/O Mode SPI Serial FLASH Serial Data Input (RTL8370N-VB output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
SPI_F_CLK/P7LED2	67	I/O_{PU}	8	SPI FLASH Clock.

7.6. Configuration Strapping Pins

Table 7. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
STRP_EEPROM_MOD/ P4LED0	80	I/O_{PU}	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16). *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*

Pin Name	Pin No.	Type	Description
STRP_EN_PWRLIGHT/ P3LED2	83	I/O$_{PU}$	Enable LED Power On Light. Pull Up: Enable LED Power On Light upon power on or reset Pull Down: Disable LED Power On Light upon power on or reset *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
STRP_EN_FLASH/ P3LED0	84	I/O$_{PU}$	Enable SPI Flash Interface Pull Up: Enable SPI Flash Interface upon power on or reset Pull Down: Disable SPI Flash Interface upon power on or reset *Note 1: Please Refer chapter 7.7 for detail description.* *Note 2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
STRP_DIS_8051/P2LED2	85	I/O$_{PU}$	Disable Embedded 8051. Pull Up: Disable embedded 8051 upon power on or reset Pull Down: Enable embedded 8051 upon power on or reset *Note 1: Please Refer chapter 7.7 for detail description.* *Note 2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
STRP_DISAUTOLOAD/ P2LED0	86	I/O$_{PU}$	Disable EEPROM or SPI FLASH Auto download. Pull Up: Disable EEPROM or SPI FLASH auto download upon power on or reset Pull Down: Enable EEPROM or SPI FLASH auto download upon power on or reset *Note1: Please Refer chapter 7.7 for detail description.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
STRP_SMI_SEL_1/ P1LED2 STRP_SMI_SEL_0/ P0LED0	88 94	I/O$_{PU}$ I/O$_{PU}$	External CPU Access Interface Selection. STRP_SMI_SEL[1:0]: 00：LSB I^2C mode 01：MSB I^2C mode 10：Slave MII Management MDC/MDIO 11：Realtek I^2C-like mode *Note: These pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*

Pin Name	Pin No.	Type	Description
STRP_MID29/P1LED0	89	I/O_{PU}	Select Slave MII Management MDC/MDIO Device ID. Pull Down: MDC/MDIO DEVID=0 *upon power on or reset* Pull Up: MDC/MDIO DEVID=29 upon power on or reset *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
STRP_EN_EEE/P1LED1	90	I/O_{PU}	EEE enable/disable Pull Up: Enable MAC/PHY 100Base-T & 1000Base-TX EEE upon power on or reset Pull Down: Disable MAC/PHY 100Base-T & 1000Base-TX EEE upon power on or reset *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*
STRP_EN_PHY/P0LED2	91	I/O_{PU}	Enable Embedded PHY. Pull Up: Enable embedded PHY upon power on or reset Pull Down: Disable embedded PHY upon power on or reset *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.*

7.7. Configuration Strapping Pins (STRP_DISAUTOLOAD, STRP_DIS_8051, STRP_EN_FLASH)

Table 8. Configuration Strapping Pins (STRP_DISAUTOLOAD, STRP_DIS_8051, STRP_EN_FLASH)

STRP_DISAUTOLOAD	STRP_DIS_8051	STRP_EN_FLASH	Initial Stage (Power On or Reset) Loading Data	
			From	To
0	0	0	EERPOM	Embedded 8051 Instruction Memory
0	0	1	SPI FLASH	Embedded 8051 Instruction Memory
0	1	0	EEPROM	Register
1	Irrelevant	Irrelevant	Do Nothing	Do Nothing

7.8. Miscellaneous Pins

Table 9. Test Pins

Pin Name	Pin No.	Type	Description
XTALI	98	AI	25MHz Crystal Clock Input Pin. 25MHz +/-50ppm tolerance crystal reference input.
XTALO	97	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.
MDIREF	17	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
GPIO8	65	I/O_{PU}	General Purpose Input/Output Interfaces IO8.
GPIO9	66	I/O_{PU}	General Purpose Input/Output Interfaces IO9.
GPIO1/P6LED0	71	I/O_{PU}	General Purpose Input/Output Interfaces IO1.
GPIO7/P6LED1	72	I/O_{PU}	General Purpose Input/Output Interfaces IO7.
GPIO0/P5LED2	73	I/O_{PU}	General Purpose Input/Output Interfaces IO0.
GPIO3/P4LED2	79	I/O_{PU}	General Purpose Input/Output Interfaces IO3.
GPIO6/P4LED1	81	I/O_{PU}	General Purpose Input/Output Interfaces IO6.
GPIO5/P3LED1	82	I/O_{PU}	General Purpose Input/Output Interfaces IO5.
GPIO4/P2LED1	87	I/O_{PU}	General Purpose Input/Output Interfaces IO4.
GPIO2/P0LED2	91	I/O_{PU}	General Purpose Input/Output Interfaces IO2.
SCK/MMD_MDC	100	I/O_{PU}	EEPROM I^2C Host Interface Clock/Slave I2C-like Interface Clock/Slave MII Management Interface Clock
SDA/MMD_MDIO	101	I/O_{PU}	EEPROM I^2C Host Interface Data/Slave I2C-like Interface Data/Slave MII Management Interface Data
nRESET	99	I_S	System Reset Input Pin. When low active will reset the RTL8370N-VB.

7.9. Test Pins

Table 10. Test Pins

Pin Name	Pin No.	Type	Description
ATESTCK0	123	AO	Reserved for Internal Use. Must be left floating.

7.10. Power and GND Pins

Table 11. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO	77	P	Digital I/O High Voltage Power.
DVDDL	20, 21, 22, 23, 76, 78, 92, 95	P	Digital Low Voltage Power.

Pin Name	Pin No.	Type	Description
AVDDH	5, 15, 19, 24, 34, 54, 64, 96, 102, 112	AP	Analog High Voltage Power.
AVDDL	10, 18, 29, 39, 49, 59, 107, 117, 128	AP	Analog Low Voltage Power.
PLLVDDL0	122	AP	PLL0 Low Voltage Power.
PLLVDDL1	44	AP	PLL1 Low Voltage Power.
GND	EPAD	G	GND.
AGND	16	AG	Analog GND.

8. Physical Layer Functional Overview

8.1. MDI Interface

The RTL8370N-VB embeds eight Gigabit Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-Tx, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

8.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

8.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

8.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

8.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

8.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

8.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

8.8. Auto-Negotiation for UTP

The RTL8370N-VB obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8370N-VB advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

8.9. Crossover Detection and Auto Correction

The RTL8370N-VB automatically determines whether or not it needs to crossover between pairs (see Table 12) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8370N-VB automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 12. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
D	D	Unused	Unused	C	Unused	Unused

8.10. Polarity Correction

The RTL8370N-VB automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

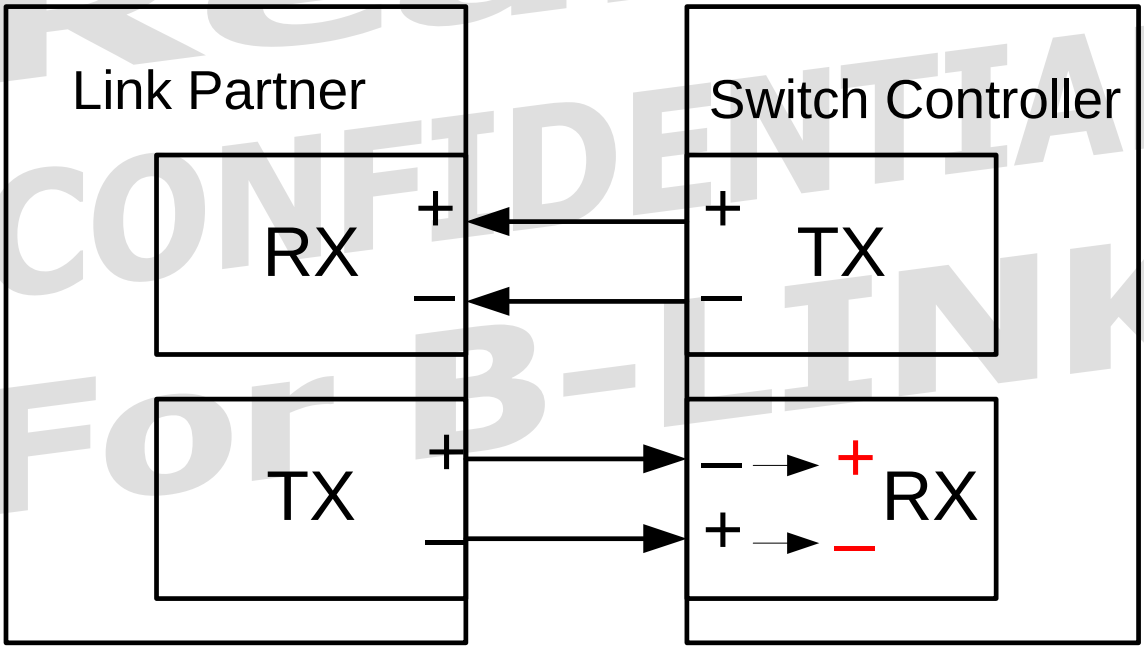


Figure 4. Conceptual Example of Polarity Correction

9. General Function Description

9.1. Reset

9.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8370N-VB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

9.1.2. Software Reset

The RTL8370N-VB supports two software resets; a chip reset and a soft reset.

9.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

9.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will clear the FIFO and re-start the packet buffer link list.

9.2. IEEE 802.3x Full Duplex Flow Control

The RTL8370N-VB supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

9.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the

medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "truncated binary exponential backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8370N-VB is 9.

The half duplex back-off algorithm in the RTL8370N-VB does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

9.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8370N-VB sends a 12-byte jam pattern (preamble+SFD+4bytes 0xAA) to collide with incoming packets when congestion control is activated. RTL8370N-VB supports 48PASS1 function, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

9.4. Search and Learning

Search

When a packet is received, the RTL8370N-VB uses the destination MAC address, Filtering Identifier (FID) and enhanced Filtering Identifier (FID) to search the 4096-entry look-up table. The 48-bit MAC address, 12-bit FID and 3-bit EFID use a hash algorithm to calculate an 11-bit index value. The RTL8370N-VB uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8370N-VB uses the source MAC address, FID, and EFID of the incoming packet to hash into a 11-bit index. It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8370N-VB will update the entry with new information. If there is no match and the 4096 entries are not all occupied by other MAC addresses, the RTL8370N-VB will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding

source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8370N-VB is between 200 and 400 seconds (typical is 300 seconds).

9.5. SVL and IVL/SVL

The RTL8370N-VB supports a 4K-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

9.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length>maximum length) will be discarded by the RTL8370N-VB. The maximum packet length may be set to 1522, 1536, 1552, or 16384 bytes.

9.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8370N-VB supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 13 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 13. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
All LANs Bridge Management Group Address	01-80-C2-00-00-10
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined 802.1 Bridge Address	01-80-C2-00-00-04 | 01-80-C2-00-00-0F
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F

9.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8370N-VB enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate, all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

9.9. Port Security Function

The RTL8370N-VB supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

9.10. MIB Counters

The RTL8370N-VB supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

9.11. Port Mirroring

The RTL8370N-VB supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored from a mirror port.

9.12. VLAN Function

The RTL8370N-VB supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to ‘Admit All’ or ‘Admit All Tagged’
- ‘Admit’ or ‘Discard’ frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8370N-VB will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8370N-VB also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In embedded system applications, CPU may want to know which input port this packet came from. The RTL8370N-VB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8370N-VB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

9.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an I2C-like Slave or Slave MII Management interface. The 4096-entry VLAN Table designed into the RTL8370N-VB provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

9.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8370N-VB supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8370N-VB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8370N-VB compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8370N-VB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8370N-VB performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8370N-VB. One is the 'VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

9.12.3. Protocol-Based VLAN

The RTL8370N-VB supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 5. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be 'Ethernet' and value to be '0x0800'. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

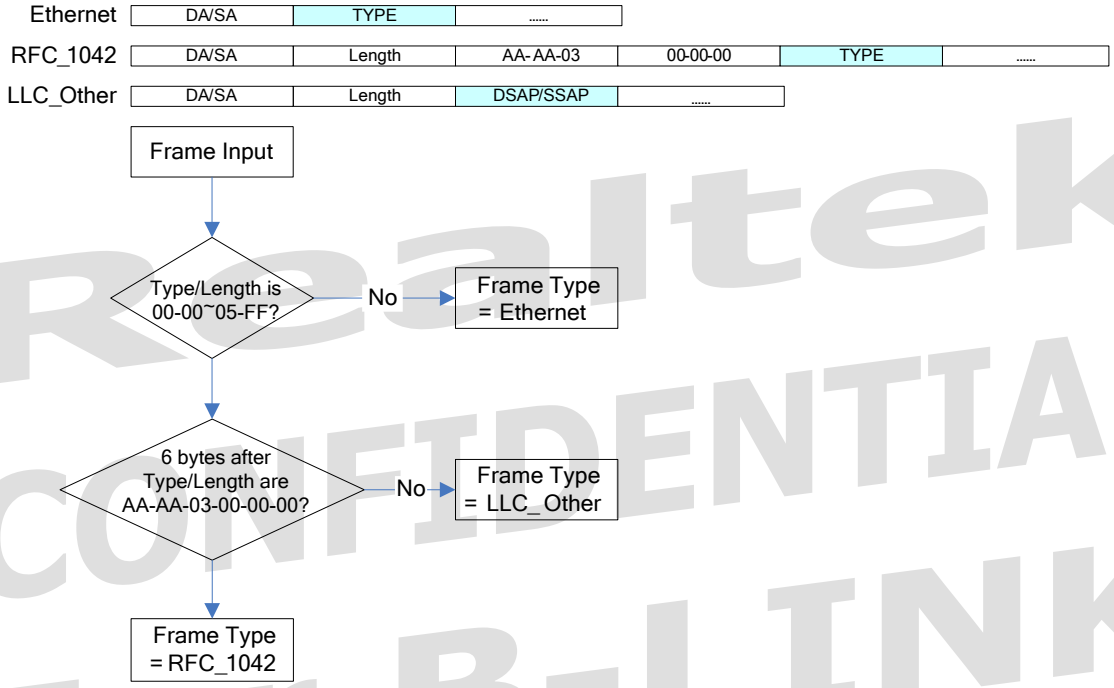


Figure 5. Protocol-Based VLAN Frame Format and Flow Chart

9.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8370N-VB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8370N-VB will drop non-tagged packets and packets with an incorrect PVID.

9.13. QoS Function

The RTL8370N-VB supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8370N-VB, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

9.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a ‘pause ON’ frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

9.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8370N-VB can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8370N-VB identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority

9.13.3. Priority Queue Scheduling

The RTL8370N-VB supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- APR leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 6 shows the RTL8370N-VB packet-scheduling diagram.

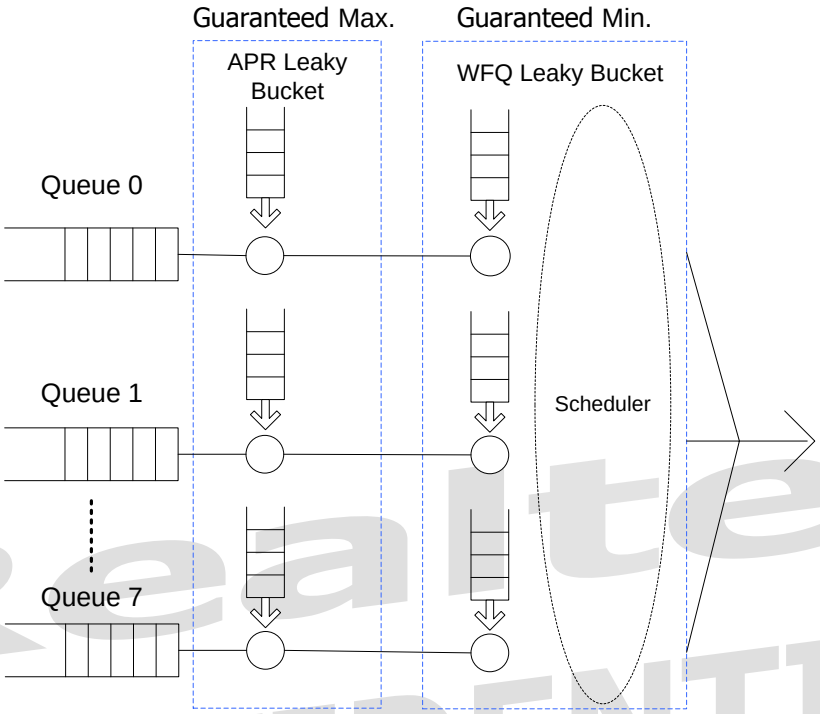


Figure 6. RTL8370N-VB MAX-MIN Scheduling Diagram

9.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8370N-VB supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 4 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. Each output queue has a 3-bit 802.1p/Q, and a 6-bit IP DSCP value configuration register.

9.13.5. ACL-Based Priority

The RTL8370N-VB supports 64-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

9.14. IGMP & MLD Snooping Function

The RTL8370N-VB can trap all IGMP and MLD packets to the CPU port. The CPU processes these packets, gets the IP multicast group information of all ports, and writes the correct multicast entry to the lookup table via I2C-like Slave interface or Slave MII Management interface.

9.15. IEEE 802.1x Function

The RTL8370N-VB supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior
- Guest VLAN

9.15.1. Port-Based Access Control

Each port of the RTL8370N-VB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

9.15.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

9.15.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

9.15.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

9.15.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction must be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

9.15.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

9.15.7. Guest VLAN

When the RTL8370N-VB enables the Port-based or MAC-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, the RTL8370N-VB will drop all packets from this port.

The RTL8370N-VB also supports one Guest VLAN to allow unauthorized ports or packets to be forwarded to a limited VLAN domain. The user can configure one VLAN ID and member set for these unauthorized packets.

9.16. IIEEE 802.1D Function

When using IEEE 802.1D, the RTL8370N-VB supports 16 sets and four status for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8370N-VB also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

9.17. Embedded 8051

An 8051 MCU is embedded in the RTL8370N-VB to support management functions. The 8051 MCU can access all of the registers in the RTL8370N-VB through the internal bus. With the Network Interface Circuit (NIC) acting as the data path, the 8051 MCU connects to the switch core and can transmit frames to or receive frames from the Ether network. The features of the 8051 MCU are listed below:

- 256 Bytes fast internal RAM
- On-chip 48K data memory
- On-chip 16K code memory
- Supports code-banking

- 12KBytes NIC buffer
- EEPROM read/write ability

9.18. Realtek Cable Test (RTCT)

The RTL8370N-VB physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open or impedance mismatch in each differential pair. The RTL8370N-VB also provides LED to indicate test status and results.

9.19. LED Indicator

The RTL8370N-VB supports parallel mode LEDs, scan mode LEDs and serial mode LEDs for each port. Each port has three LED indicators, LED0, LED1 and LED2. Each may have different indicator information (defined in Table 14). Upon reset, the RTL8370N-VB supports chip diagnostics and LED operation test by blinking all LEDs once.

Table 14. LED Definitions

LED Statuses	Description
LED_Off	LED always off.
Dup/Col	Duplex/Collision, Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

9.19.1. Parallel LED Mode

The RTL8370N-VB supports parallel LED mode. The parallel LED pin also supports pin strapping configuration functions. The PnLED0, PnLED1 and PnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is pulled high upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The PnLED1 can be combined with PnLED0 or PnLED2 as a Bi-color LED.

LED_PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

- P0LED1 should pull up upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- P0LED1 should be pulled down upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

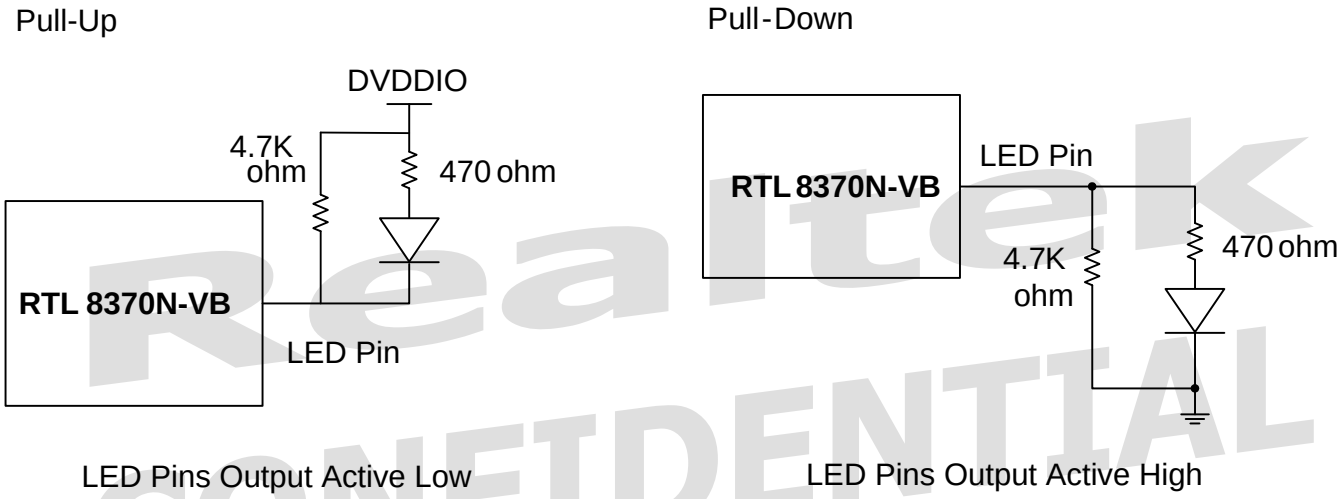


Figure 7. Pull-Up and Pull-Down of LED Pins for Single-Color LED

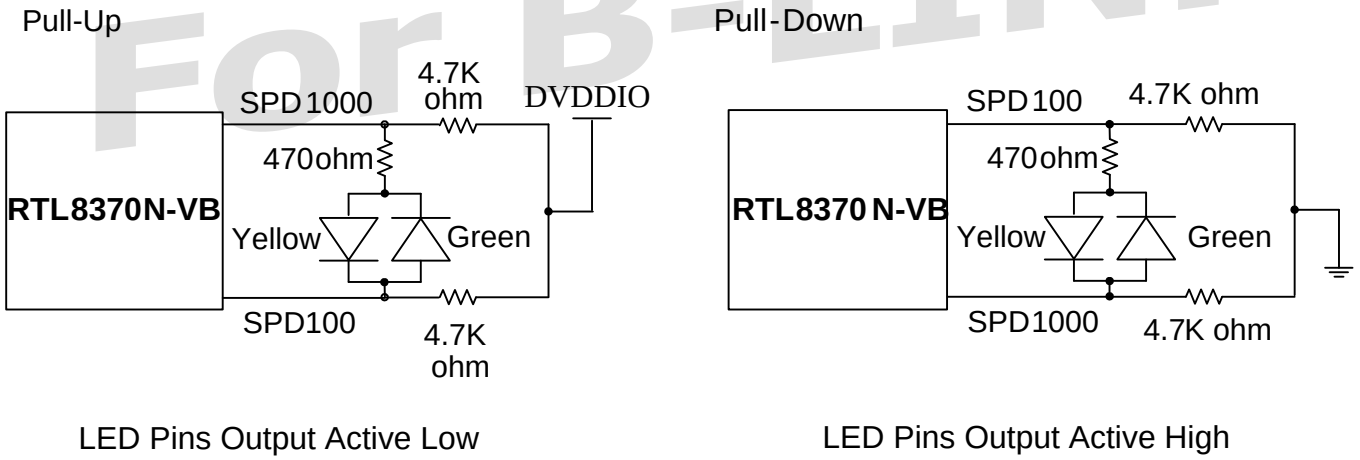


Figure 8. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

9.19.2. Scan LED Mode

The RTL8370N-VB provides scan LED mode to reduce LED pins but keep the same number of LED indicators as parallel LED mode. Each port includes one bi-color and one single-color LED. The bi-color LED consists of LED1 & LED 2 (Figure 10) and the single-color LED is driven by LED0 (Figure 9).

In the bi-color LED circuit, the 30K ohm parallel connected resistor must be used if the strapping pin on either side of the bi-color LED is pulled low. Otherwise it is not required. Some Scan mode LED pins also support strapping pins and will not affect the LED polarity.

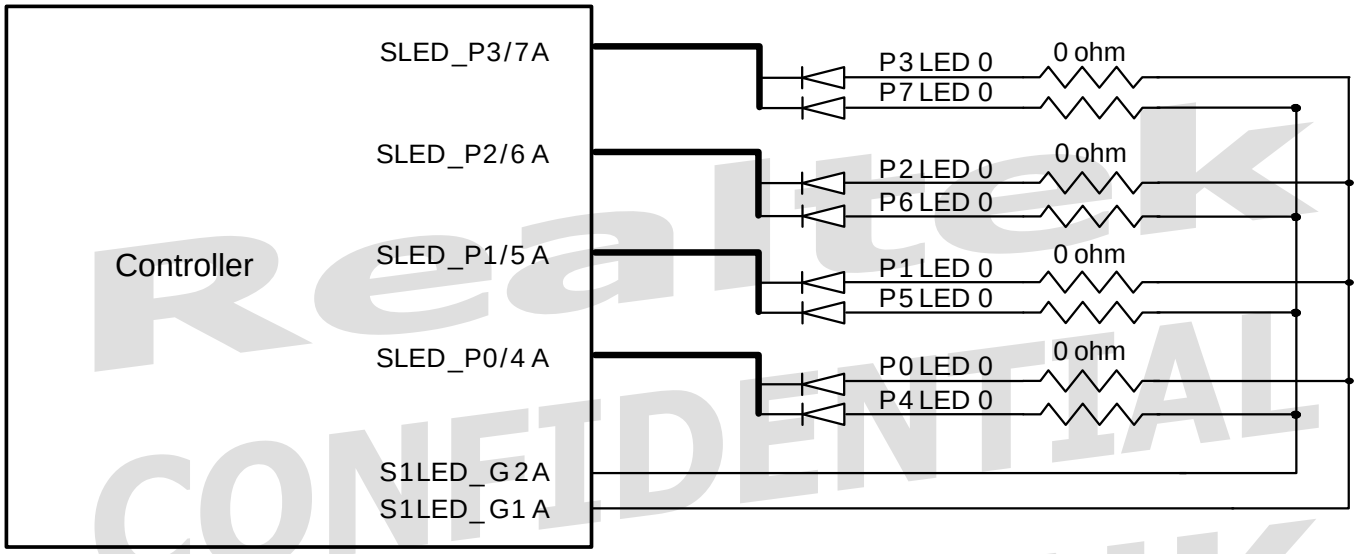


Figure 9. Scan Mode LED Connection Diagram (Group A: Single-Color LED (LED0))

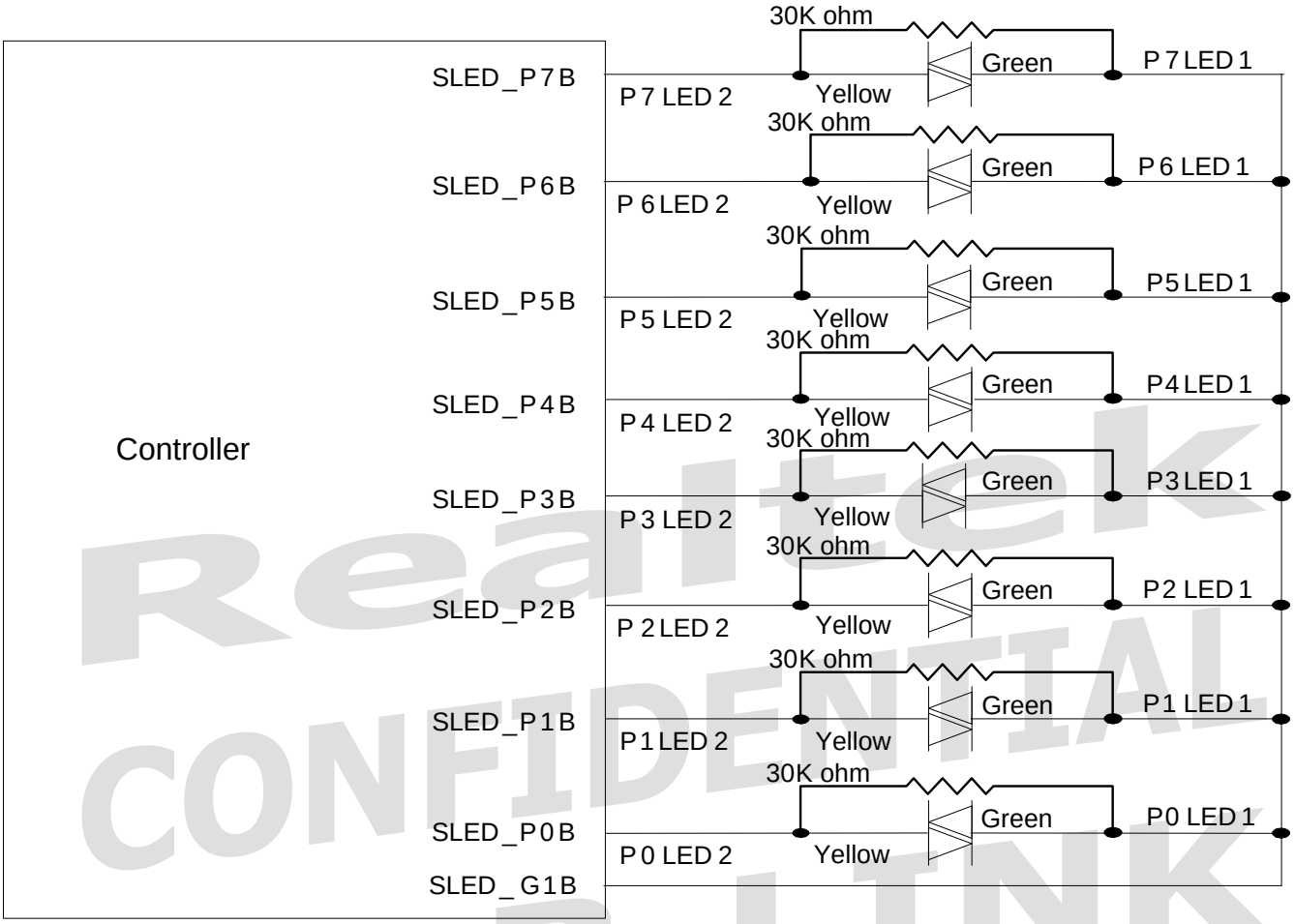


Figure 10. Scan Mode LED Connection Diagram (Group B: Bi-Color LED (LED1 & LED2))

9.19.3. Serial LED Mode

The RTL8370N-VB supports serial shift LED mode to show the speed, link status and other information of the port status.

In serial led mode, the RTL8370N-VB supports per-port one/two/three single-color LED. The serial LED default is per-port three single-color LED, and the RTL8370N-VB support 8-port (port0~port7) LED.

9.19.3.1 *Serial Shift LED Default Mode, per-port three single-color LED*

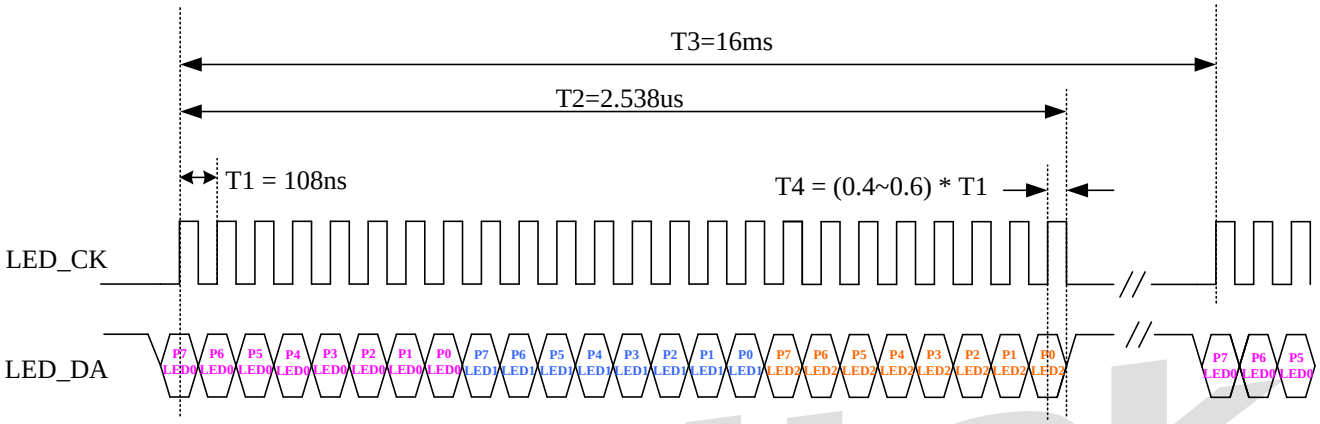


Figure 11. RTL8370N-VB serial led mode shift sequence (per-port three single-color LED)

A 74HC164 8-Bit Serial-In, Parallel-Out Shift Register captures the per-port link status and diagnostic information. The related circuit design is shown in the following diagram.

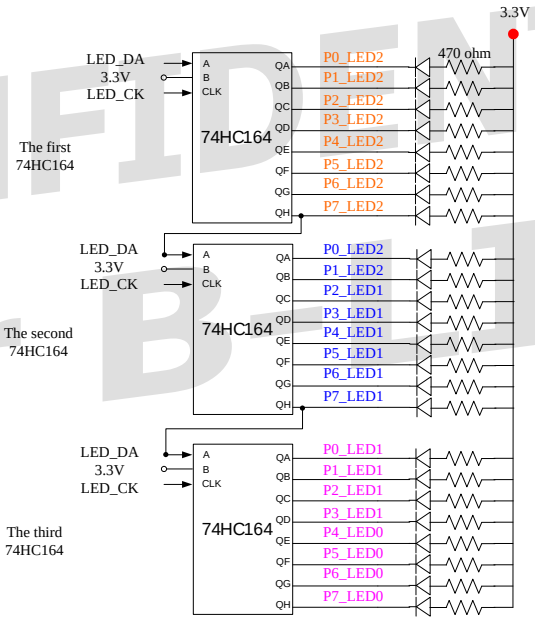


Figure 12. RTL8370N-VB+74HC164 Serial LED Connection Diagram (per-port three single-color LED)

The RTL8231 shift register mode could reserve the serial data, and output parallel data in order. There are 36 shift registers in the RTL8231. The output data sequence is shown below:

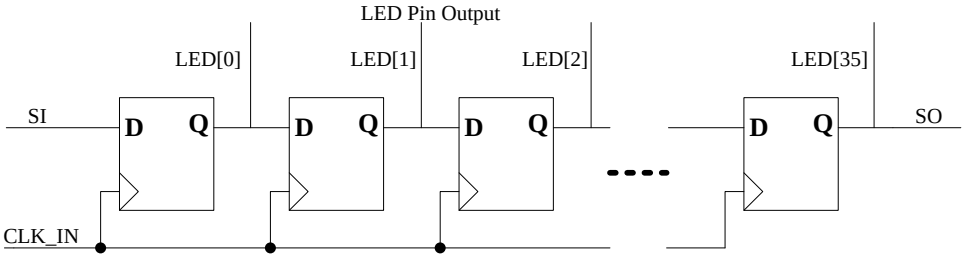


Figure 13. RTL8370N-VB+74HC164 Serial LED Connection Diagram (per-port three single-color LED)

To latch the currently serial data which receive at the SI pin and shift the preceding data to the next stage at the each rising edge of the serial clock. At the first the serial data input the RTL8231 output from the pin 15 LED[0]. At the last shift register, the serial data output to LED[35] pin and the SO pin at the same time.

The strapping pins configuration of RTL8231 in Shift Register Mode is depicted in Table 15.

Table 15. RTL8231 Shift Register Mode Strapping Pins Configuration

Pin Name	Pin Num	Type	Description	Configuration for serial LED mode
LED[0]/Dis_SMI	15	I/O_{PD}	Select RTL8231 in the SMI mode or Shift Register mode. 0: SMI mode.(default) 1: Shift register mode.	Pull high
SO/MOD[1]	16	I/O	MOD[1:0] defines the parallel output initial value after finish reset. 2b'00: LED[15] initial high, others parallel output initial low. 2b'01: all parallel output initial high. 2b'10: LED[0] initial high, others parallel output initial low. 2b'11: LED[15] initial low, others parallel output initial high.	Pull low
LED[15]/MOD[0]	42	I/O_{PU}		Pull high

9.19.3.2 Serial Shift LED, per-port two single-color LED

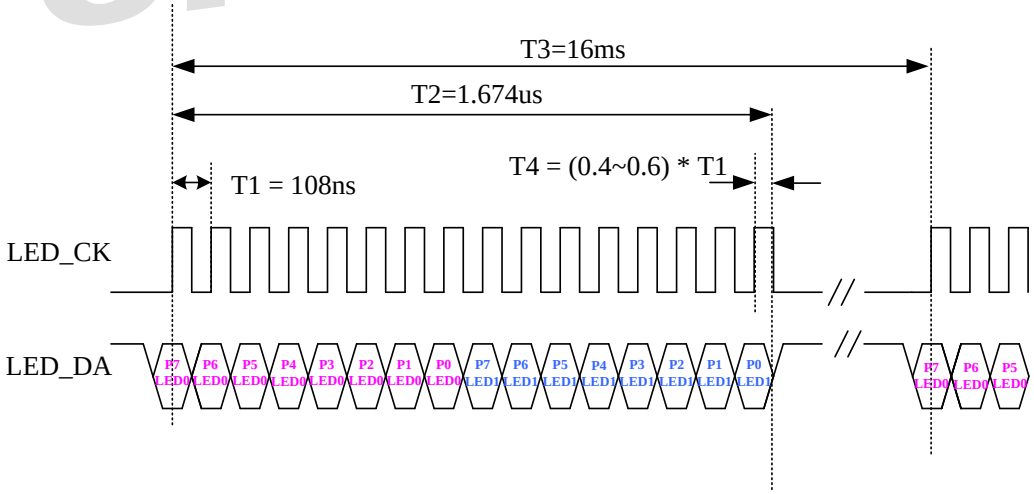


Figure 14. RTL8370N-VB serial led mode shift sequence (per-port two single-color LED)

9.19.3.3 Serial Shift LED, per-port one single-color LED

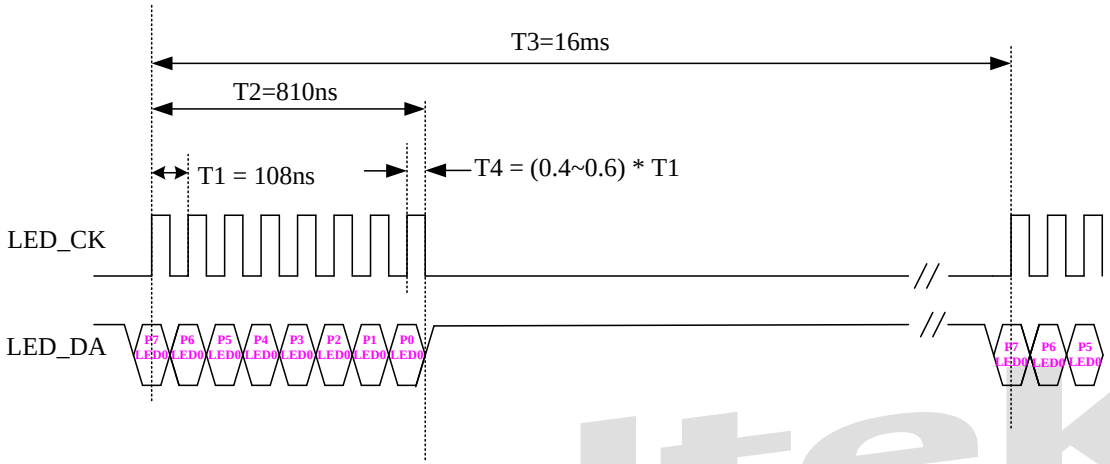


Figure 15. RTL8370N-VB serial led mode shift sequence (per-port one single-color LED)

9.20. Green Ethernet

9.20.1. Link-On and Cable Length Power Saving

The RTL8370N-VB provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

9.20.2. Link-Down Power Saving

The RTL8370N-VB implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

9.21. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8370N-VB support IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation, and 10Base-T in full/half duplex mode.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access

Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL8370N-VB MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

10. Interface Descriptions

10.1. I²C Master for EEPROM Auto-load

The EEPROM interface of the RTL8370N-VB uses the serial bus I²C to read the Serial EEPROM. When the RTL8370N-VB is powered up, it drives SCK and SDA to read the configuration/code data from the EEPROM by strapping configuration.

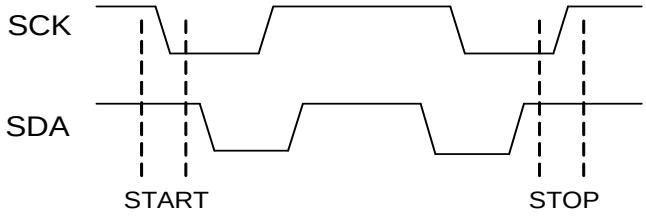


Figure 16. I2C Start and Stop Command

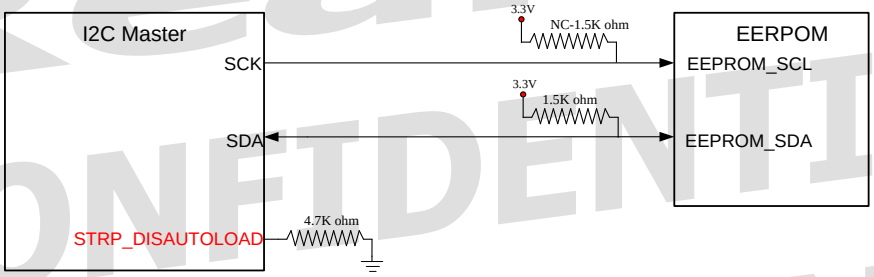


Figure 17. I2C Master for EEPROM Auto-load Interface Connection Example

The EEPROM can be divided into two sizes: 2Kb~16Kb and 32Kb~512Kb. The address of the small size EEPROM is 8-bits, however the larger EEPROM has word-high addressing and word-low addressing, and it is 16-bits (two bytes). The RTL8370N-VB supports these two types EEPROM.

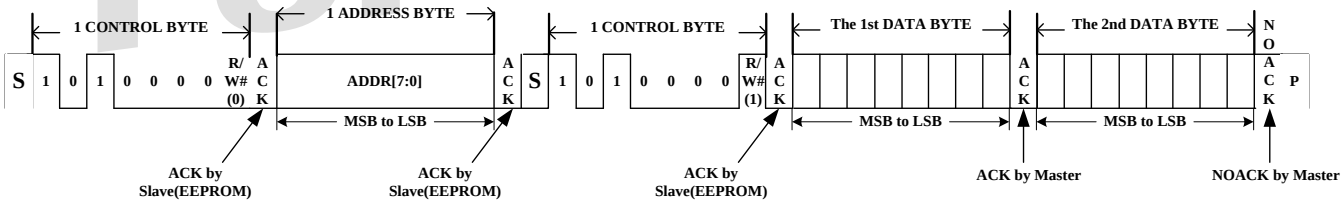


Figure 18. 8-Bit EEPROM Sequential Read

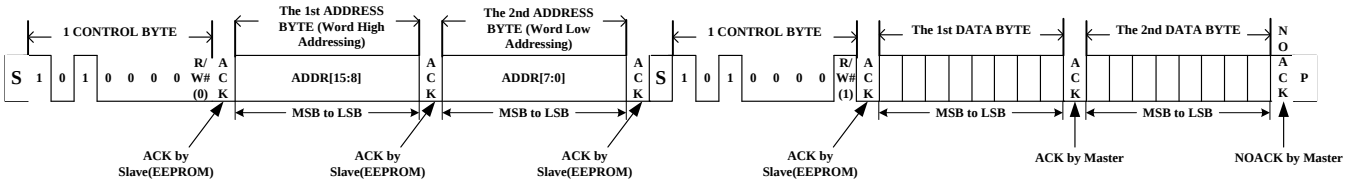


Figure 19. 16-Bit EEPROM Sequential Read

10.2. I²C-Like Slave Interface for External CPU to Access RTL8370N-VB

When EEPROM auto-load is completed, the RTL8370N-VB registers can be accessed via SCK and SDA (I²C-Like) via an external CPU (Decided by Strapping Configuration).

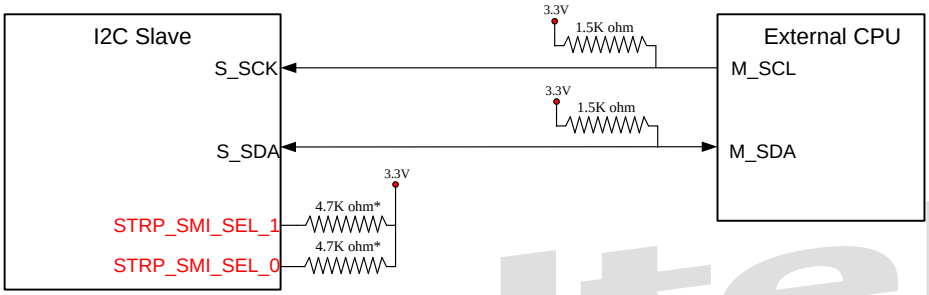


Figure 20. I2C-Like Slave for External CPU Access Interface Connection Example

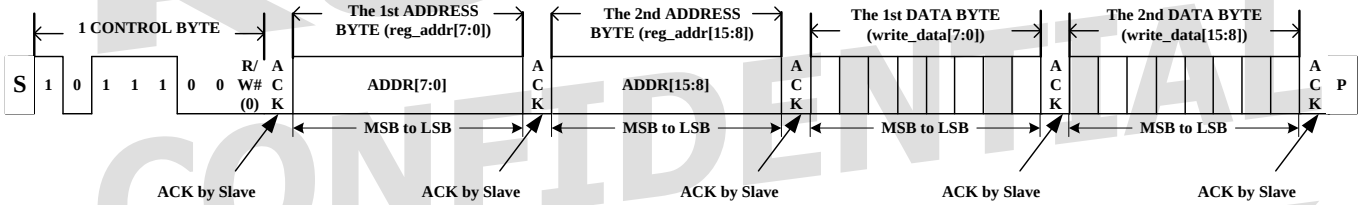


Figure 21. I2C-Like Slave Interface Write Command

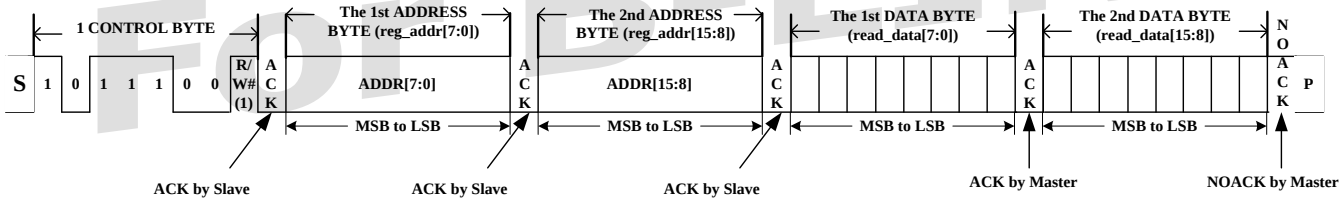


Figure 22. I2C-Like Slave Interface Read Command

10.3. Slave MII Management SMI Interface for External CPU to Access RTL8370N-VB

The RTL8370N-VB registers can be accessed via Slave MDC and MDIO via an external CPU (Decided by Strapping Configuration).

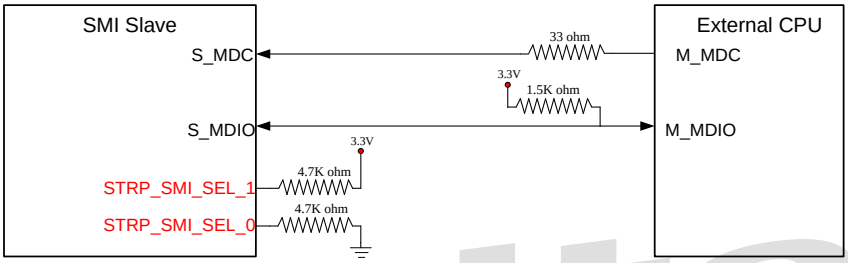


Figure 23. Slave MII Management SMI Interface Connection Example

Table 16. Slave MII Management SMI Access Format

	Management Frame Fields							
	PRE	**ST**	**OP**	**DEVAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note: The Slave needs no less than 32bit Preambles (PRE) for accessing slave by Slave SMI interface default. External CPU can configure the Slave to enable preamble suppression function, and then the Slave doesn't need preamble for accessing slave.

10.4. SPI FLASH Interface

The RTL8370N-VB supports Serial IO and Dual IO mode SPI Interface to Connect SPI FLASH. The RTL8370N-VB only supports 3-byte address mode access. No more than 4Mbyte capacity of the SPI FLASH is better for RTL8370N-VB application.

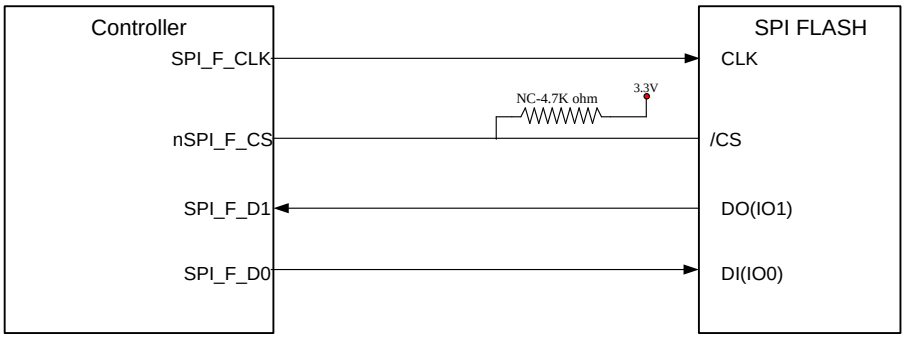


Figure 24. SPI FLASH Interface Connection Example

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 17. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO_2, DVDDIO_0, DVDDIO_1, AVDDH, Supply Referenced to GND and AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1 Supply Referenced to GND, AGND, PLLGND0, and PLLGND1	GND-0.3	+1.21	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

11.2. Recommended Operating Range

Table 18. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDDIO, AVDDH Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1 Supply Voltage Range	1.045	1.1	1.155	V

11.3. Thermal Characteristics

11.3.1. LQFP-128-EPAD

11.3.1.1 Assembly Description

Table 19. Assembly Description

Package	Type	E-Pad LQFP128
	Dimension (L x W)	14 x 20 mm
	Thickness	1.4 mm
PCB	PCB Dimension (L x W)	130 x 75mm
	PCB Thickness	1.6 mm

	Number of Cu Layer-PCB	2-Layer: - Top layer (1oz): 20% coverage of Cu - Bottom layer (1oz): 75% coverage of Cu 4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

11.3.1.2 Material Properties

Table 20. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.88
PCB		Cu	400
		FR4	0.2

11.3.1.3 Simulation Conditions

Table 21. Simulation Conditions

Input Power	2.6W
Test Board (PCB)	2L (2S)/4L (2S2P)
Control Condition	Air Flow = 0, 1, 2 m/s

11.3.1.4 Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convection

Table 22. Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	18.2	8.2	7.5	2.5	8.8
2L PCB	30.1	10.0	8.9	3.4	11

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB}: Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JT}: Junction to top center of package thermal characterization
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

11.3.1.5 *Thermal Performance of E-Pad LQFP-128 on PCB under Forced Convection*

Table 23. Thermal Performance of E-Pad LQFP-128 on PCB under Forced Convection

	Air Flow (m/s)	0	1	2
4L PCB	θ_{JA}	18.2	15.2	14.2
	Ψ_{JT}	2.5	2.8	3.5
	Ψ_{JB}	8.8	8.6	8.3
2L PCB	θ_{JA}	30.1	25.9	24.2
	Ψ_{JT}	3.4	4.5	5.6
	Ψ_{JB}	11	10.7	10.5

11.4. DC Characteristics

Table 24. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
System Idle (No UTP Port Link Up, 1 System Power LED)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	41	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	165	-	mA
Total Power Consumption for All Ports	PS	-	316.8	-	mW
1000M Active (8 UTP Ports Link Up, 1 System Power LED, 8 Activity LEDs, 8 Speed LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	530	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	881	-	mA
Total Power Consumption for All Ports	PS	-	2718.1	-	mW
100M Active (8 UTP Ports Link Up, 1 System Power LED, 8 Activity LEDs, 8 Speed LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	201	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	282	-	mA
Total Power Consumption for All Ports	PS	-	973.5	-	mW
10M Active (8 UTP Ports Link Up, 1 System Power LED, 8 Activity LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	242	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	200	-	mA
Total Power Consumption for All Ports	PS	-	1020	-	mW
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	1.9	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V
Output Low Voltage	V_{ol}	-	-	0.4	V

Note1: DVDDIO=3.3V, AVDDH=3.3V, DVDDL=1.1V, AVDDL=1.1V PLLVDDL=1.1V.

11.5. AC Characteristics

11.5.1. I²C Master for EEPROM Auto-load Interface Timing Characteristics

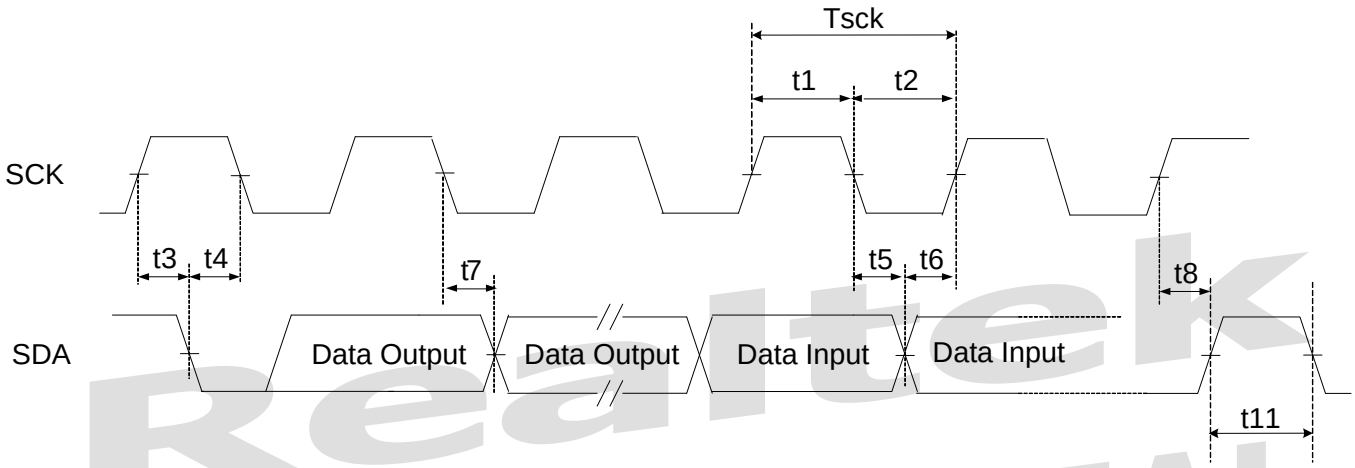


Figure 25. Master I2C for EEPROM Auto-load Timing Characteristics

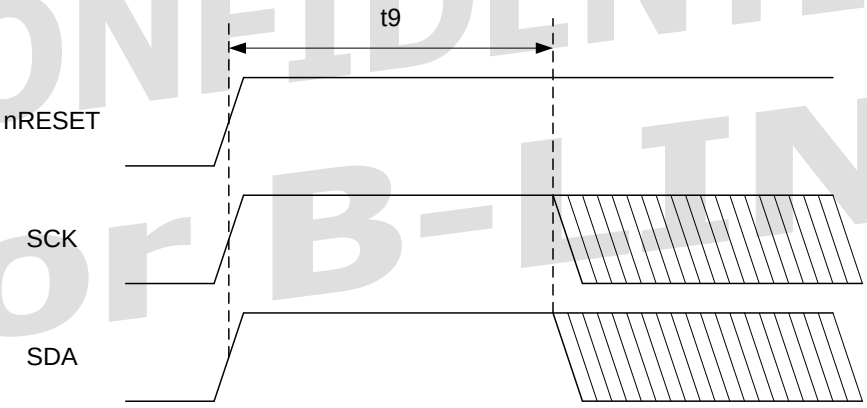


Figure 26. Master I2C for EEPROM Auto-load Power on Timing

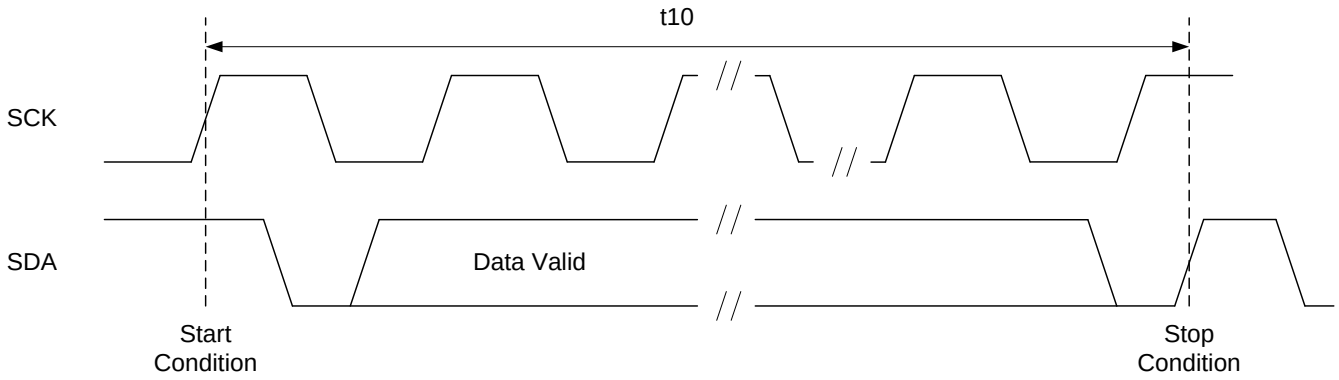


Figure 27. Master I2C for EEPROM Auto-load Timing

Table 25. Master I2C for EEPROM Auto-load Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
Tsck	SCK Clock Period	O		9	-	µs
t1	SCK High Time	O	4.05	4.5	-	µs
t2	SCK Low Time	O	4.05	4.5	-	µs
t3	START Condition Setup Time	O	2		-	µs
t4	START Condition Hold Time	O	2		-	µs
t5	Data Input Hold Time	I	0		-	ns
t6	Data Input Setup Time	I	10		-	ns
t7	Data output delay	O	2.15		2.35	µs
t8	STOP Condition Setup Time	O	2		-	µs
t9	SCK/SDA Active from Reset Ready	O	-	76.8	-	ms
t10	8K-bits EEPROM Auto-Load Time	O	-	236	-	ms
t11	Time the bus free before new START	O	10			µs
-	SCK Rise Time (10% to 90%)	O	-		100	ns
-	SCK Fall Time (90% to 10%)	O	-		100	ns
-	Duty Cycle	O	40	50	60	%

Note: t9, and t10 are measured with the ATMEL AT24C08 EEPROM.

11.5.2. RTK I²C-Like Slave Mode for External CPU Access Interface Timing Characteristics

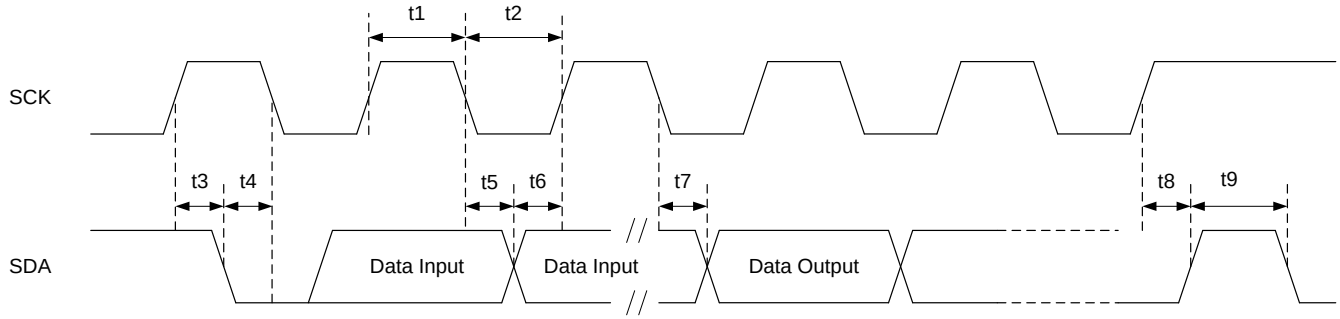


Figure 28. RTK Slave I2C-Like for External CPU Access Interface Timing Characteristics

Table 26. Slave I2C-Like for External CPU Access Interface Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	4.0	-	-	µs
t2	SCK Low Time	I	4.0	-	-	µs
t3	START Condition Setup Time	I	0.25	-	-	µs
t4	START Condition Hold Time	I	0.25	-	-	µs
t5	Data Input Hold Time	I	0	-	-	µs
t6	Data Input Setup Time	I	100	-	-	ns
t7	Clock to Data Output Delay	O	10	-	100	ns
t8	STOP Condition Setup Time	I	0.25	-	-	µs
t9	Time the bus free before new START	I	0.5			µs

11.5.3. Slave MII Management SMI for External CPU Access Interface Timing Characteristics

The RTL8370N-VB supports MDIO slave mode. The Master (the RTL8370N-VB link partner CPU) can access the Slave (RTL8370N-VB) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the Master sources the MDIO signal. In a read command, the Slave sources the MDIO signal.

- The timing characteristics of the Master (the RTL8370N-VB link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics of the Slave (RTL8370N-VB) are provided by the RTL8370N-VB when the RTL8370N-VB sources the MDIO signal (Read command)

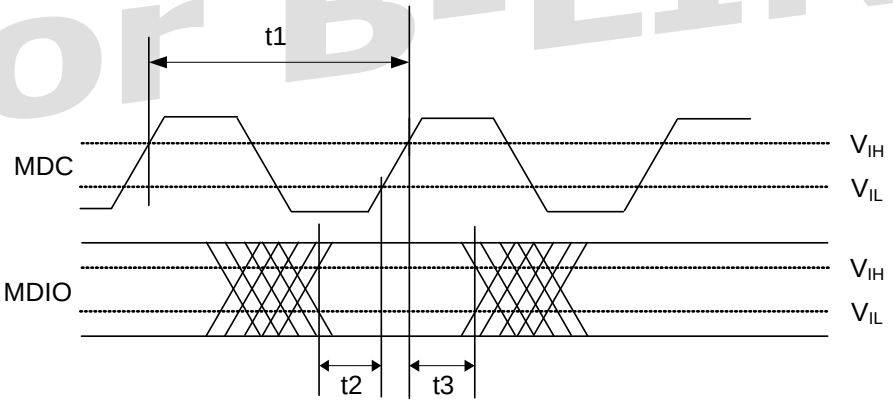


Figure 29. MDIO Sourced by Master (External CPU)

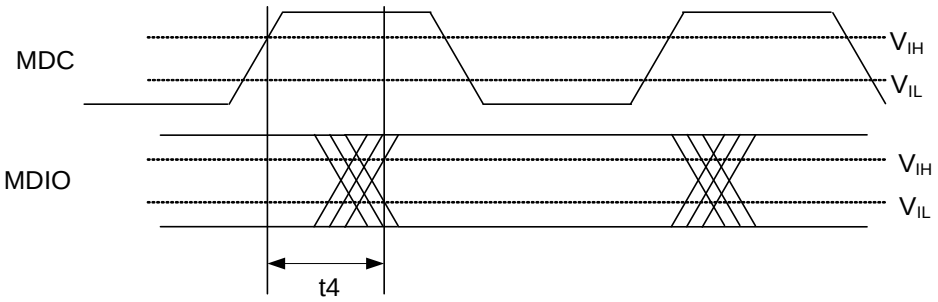


Figure 30. MDIO Sourced by Slave (RTL8370N-VB)

Table 27. Slave SMI (MDC/MDIO) Timing Characteristics and Requirements

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	8	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	8	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Rising Edge) to Data Delay Time	O	0	-	80	ns

11.5.4. Serial Shift Mode LED Interface Timing Characteristics

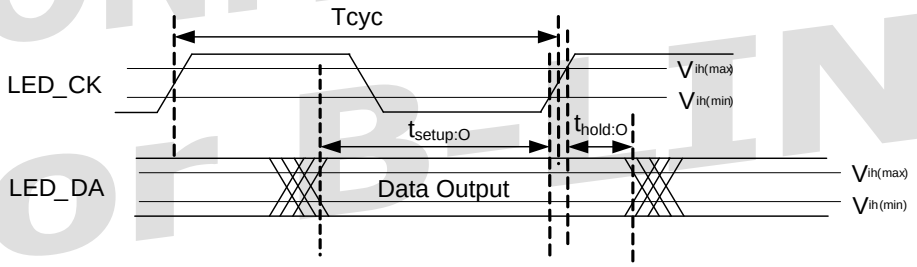


Figure 31. Serial Shift Mode LED Timing Characteristics

Table 28. Serial Shift Mode LED AC Timing

Mode and Description		Symbol	Min	Typical	Max	Units
Serial Shift LED	Input High Voltage	Vih	2.0	-	-	V
	Input Low Voltage	Vil	-	-	0.8	V
	LED_CK Clock Cycle	Tcyc	-	108	-	ns
	Duty Cycle of the LED_CK	Duty	45	50	55	%
	LED_DA to LED_CK Output Setup Time	$t_{setup:O}$	40	-	-	ns
	LED_DA to LED_CK Output Hold Time	$t_{hold:O}$	20	-	-	ns

11.5.5. SPI FLASH Interface Timing Characteristics

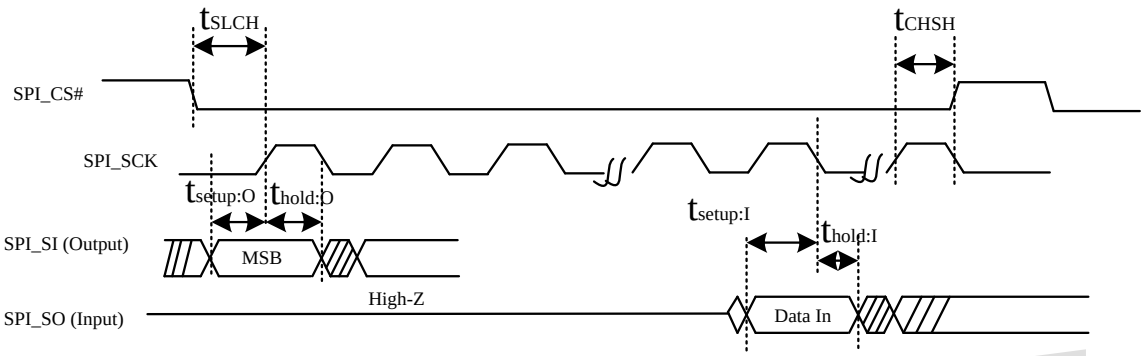


Figure 32. SPI FLASH Timing Characteristics

Table 29. SPI FLASH AC Timing

Symbol	Description	Type	Min	Typical	Max	Units
f_{SPI_SCK}	Clock Frequency of the SPI_SCK	O	-	62.5		MHz
Duty	Duty Cycle of the SPI_SCK	O	45	50	55	%
t_{SLCH}	CS# Active Setup Time	O	6	-	-	ns
t_{CHSH}	CS# Active Hold Time	O	6	-	-	ns
$t_{setup:O}$	Data Output Setup Time	O	5	-	-	ns
$t_{hold:O}$	Data Output Hold Time	O	6	-	-	ns
$t_{setup:I}$	Data Input Setup Time	I	2	-	-	ns
$t_{hold:I}$	Data Input Hold Time	I	0	-	-	ns
Test Condition: F_{SPI_SCK}=62.5MHz						

11.6. Power and Reset Characteristics

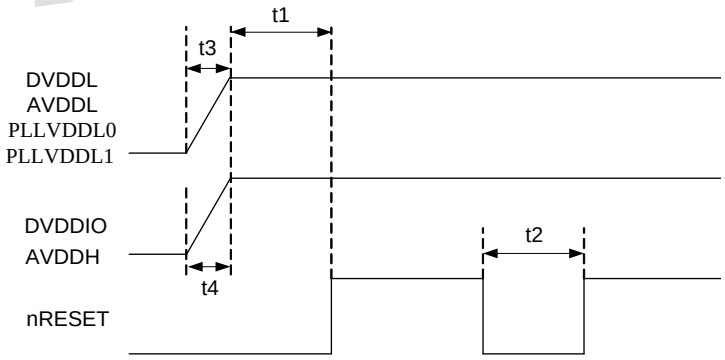


Figure 33. Power and Reset Characteristics

Table 30. Power and Reset Characteristics

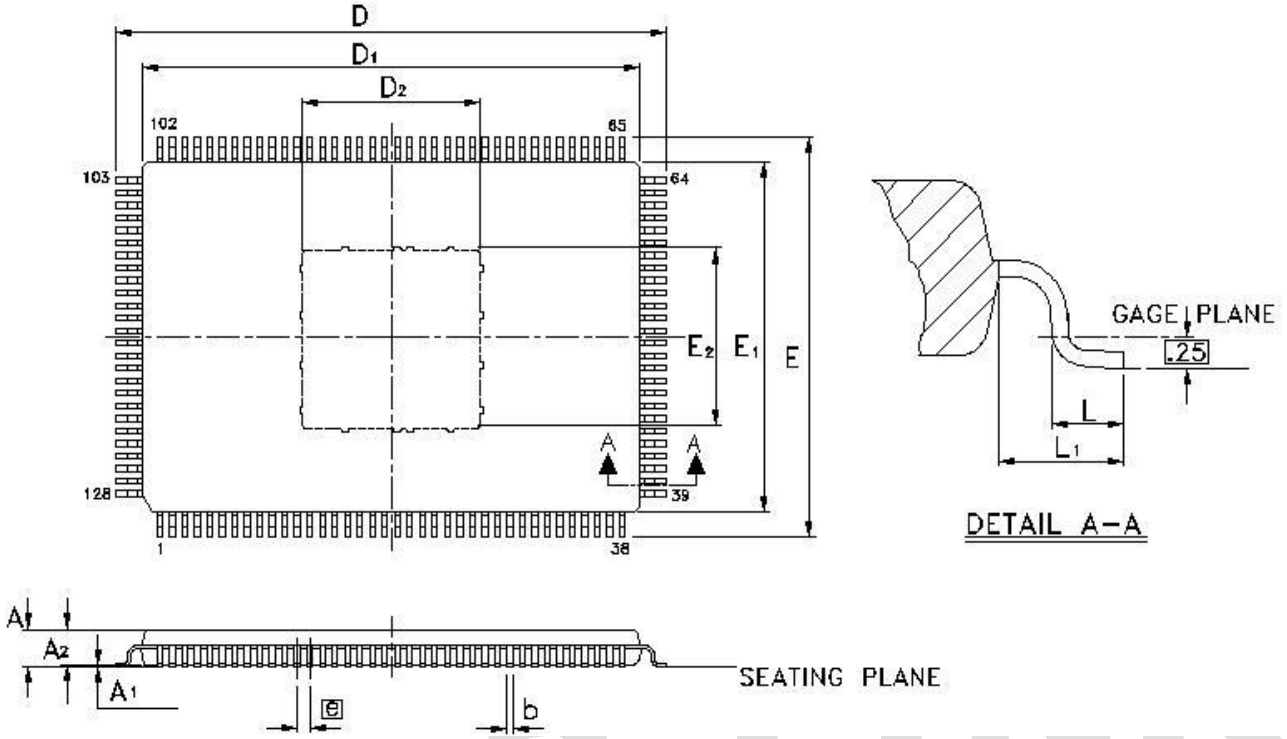
Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Reset Delay Time	t1	The duration from all powers steady to the reset signal released to high.	I	10	-	-	ms

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Reset Low Time	t2	The duration of reset signal remain low time for issuing a reset to RTL8370N-VB.	I	10	-	-	ms
VDDL Power Rising Settling Time	t3	DVDDL, AVDDL, PLLVDDL0 and PLLVDDL1 power rising settling time.	I	0.5	-	100	ms
VDDH Power Rising Settling Time	t4	DVDDIO and AVDDH power rising settling time.	I	0.5	-	100	ms

12. Mechanical Dimensions

12.1. RTL8370N-VB*: LQFP 128-Pin E-PAD Package*

Thermally Enhanced Low-profile Quad Flat Package (LQFP) 128 Leads 14x20mm Outline.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	0.15	0.002	-	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.2	0.27	0.007	0.009	0.011
D		22.00BSC			0.866BSC	
D_1		20.00BSC			0.787BSC	
D_2/E_2	5.60	6.60	7.50	0.220	0.260	0.295
E		16.00BSC			0.630BSC	
E_1		14.00BSC			0.551BSC	
e		0.50BSC			0.020BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00REF			0.039REF	

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

13. Ordering Information

Table 31. Ordering Information

Part Number	Package	Status
RTL8370N-VB-CG	LQFP 128-Pin E-PAD ‘Green’ Package	

Realtek Semiconductor Corp.
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